METHOD AND APPARATUS FOR ROUTING INTERCONNECTS TO DEVICES WITH DISSIMILAR PITCHES

FIELD OF THE INVENTION

[0001] The present invention relates generally to routing for devices with different pitch, and more particularly to routing of a core embedded in a programmable logic device where the core comprises a different pitch than the programmable logic device.

BACKGROUND OF THE INVENTION

[0002] Programmable logic devices exist as a well-known type of integrated circuit that may be programmed by a user to perform specified logic functions. There are different types of programmable logic devices, such as programmable logic arrays (PLAs) and complex programmable logic devices (CPLDs). One type of programmable logic devices, called a field programmable gate array (FPGA), is very popular because of a superior combination of capacity, flexibility and cost.

[0003] An FPGA typically includes an array of configurable logic blocks (CLBs) surrounded by a ring of programmable input/output blocks (IOBs). The CLBs and IOBs are interconnected by a programmable interconnect structure. The CLBs, IOBs, and interconnect structure are typically programmed by loading a stream of configuration data (bitstream) into internal configuration memory cells that define how the CLBs, IOBs, and interconnect structure are configured. The configuration bitstream may be read from an external memory, conventionally an external integrated circuit memory EEPROM, EPROM, PROM, and the like, though other types of memory may be used. The collective states of the individual memory cells then determine the function of the FPGA.

[0004] A recent development in FPGA technology involves providing FPGAs comprising a plurality of what are known as "standard cells." These "standard cells" are provided inside an FPGA as functional blocks and have a set height. Notably, the term "standard cell" is not to imply that any standard, de facto or otherwise, exists, as standard cell size may vary from company to company. So, for example, logic blocks, such as a flip-flop, a NAND gate, and an inverter, among other well-known logic circuits, each will lay out with a same height, but may have different lengths. This height is conventionally dependent on pitch of a company's integrated circuit process for one or more interconnect or metal layers. A standard cell may be made up of several logic blocks, each with a same height, but possibly with different lengths. Thus, each standard cell will have a same height but may have varying lengths. Standard cells may be assembled for providing interconnectivity logic or "glue logic." Thus, an FPGA may be connected to an embedded device to carry out complex tasks.

[0005] However, an embedded device or core may not have the same layout pitch as an FPGA. Moreover, FPGA exclusive routing over an embedded core further complicates routing to an embedded core. A placement and routing database used by a routing program creates routing for connecting an FPGA to an embedded core. However, non-equivalent pitch between such an FPGA and embedded core causes design rule violations. These design rule violations heretofore were addressed by manual re-routing. However, checking a design for such violations and manually re-routing can delay production by one or more months depending on complexity and number of connections between the FPGA and embedded core.

[0006] Accordingly, it would be desirable and useful to provide a layout rules for implementation in a placement and routing database that would reduce design rule violations

owing to differences in pitch between an FPGA and an embedded core.

SUMMARY OF THE INVENTION

[0007] An aspect of the present invention is a method for configuring a routing program for routing connections between an integrated circuit device and an embedded core. More particularly, a first horizontal pitch and a first vertical pitch is obtained for one of the integrated circuit device and the embedded core, and a second horizontal pitch and a second vertical pitch is obtained for the other of the integrated circuit device and the embedded core, where the first vertical pitch and the second vertical pitch are not equal. A first connection layer input, including, but not limited to, the first vertical pitch and a horizontal direction, is provided to the routing program, and a second connection layer input, including, but not limited to, the second horizontal pitch and a vertical direction, is provided to the routing program.

[0008] An aspect of the present invention is an integrated circuit device comprising a first device coupled to a second device. The first device comprises a first horizontal pitch and a first vertical pitch. The second device comprises a second horizontal pitch and a second vertical pitch. At least one interconnect layer is for coupling the first device and the second device. The interconnect layer comprises a set of pitches selected from: (i) the first vertical pitch and the second horizontal pitch, and (ii) the first horizontal pitch and the second vertical pitch.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may

be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0010] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the present invention may admit to other equally effective embodiments.

[0011] FIG. 1 is a block diagram of an exemplary embodiment of an integrated circuit comprising an FPGA, standard cells for glue logic and a microprocessor core in accordance with one or more aspects of the present invention.

[0012] FIG. 2 is a block diagram of an exemplary embodiment of integrated circuit device cores are formed on a semiconductor wafer of the prior art.

[0013] FIGS. 3A and 3B are line diagrams of respective exemplary portions of interconnect layers from the FPGA and the microprocessor core of FIG. 1.

[0014] FIG. 4 is a cross-sectional diagram of exemplary portions of the FPGA and the microprocessor core of FIG. 1.

[0015] FIG. 5 is a line diagram of an exemplary portion of an interconnect layer from the FPGA of FIG. 1 in accordance with an aspect of the present invention.

[0016] FIG. 6 is a cross-sectional diagram of an exemplary portion of the FPGA and the microprocessor core of FIG. 1.

[0017] FIG. 7 is a flow diagram of an exemplary embodiment of a process in accordance with one or more aspects of the present invention

DETAILED DESCRIPTION OF THE DRAWINGS

[0018] In the following description, numerous specific details are set forth to provide a more thorough understanding of the present invention. However, it will be apparent to one of skill in the art that the present invention may be practiced without one or more of these specific details. In other instances, well-known features

have not been described in order to avoid obscuring the present invention.

[0019] Referring to FIG. 1, there is shown a block diagram of an exemplary embodiment of an integrated circuit 100 comprising an FPGA 10 and a microprocessor core 20 in accordance with one or more aspects of the present invention. Over FPGA 10 and microprocessor core 20 is grid 14. Grid 14 is shown to indicated that a plurality of metal interconnect lines are used for connecting FPGA 10 circuitry to microprocessor core 20 circuitry. As mentioned above, standard cells 19 may be used to provide glue logic to connect FPGA circuitry 10 and microprocessor core 20 circuitry. Vias or contacts 16 are formed to provide interconnection to desired locations of such circuitry and grid 14. Notably, grid 14 may comprise a plurality of interconnect layers, as described below in more detail.

[0020] Microprocessor core 20 comprises a plurality of pins 28. Because pins may be longer than contact pads as indicated by vias 16, there is more longitudinal variability for locating vias 16 to contact such pins 28. Though pins 28 are shown as having a longitudinal or horizontal orientation, they may have a latitudinal or vertical orientation or a combination of both. However, for purposes of clarity of explanation, a horizontal orientation is described.

[0021] In an embedded process, a plurality of microprocessor cores 20 is formed on a wafer 25, as shown in the block diagram of FIG. 2. Accordingly, there may be a region 15 between a microprocessor core 20 and an FPGA 10, as shown in FIG. 1, as FPGA 10 may be formed with a different process flow than microprocessor core 20. Region 15 may comprise standard cells 19 formed of one or more logic blocks 18.

[0022] FPGA 10 is built proximal to microprocessor core 20 on a same wafer 25 or other substrate member upon which microprocessor core 20 is located. However, owing to

differences in processes, microprocessor core 20 may have a different pitch for one or more of its interconnect layers than that of FPGA 10. So, for example, suppose microprocessor core 20 was designed for a .13 micron process technology and laid out for a .57 micron horizontal and vertical pitch for its interconnect layers. And, suppose for example that FPGA 10 was designed for a .18 micron process technology and laid out for a .66 micron horizontal pitch and a .60 micron vertical pitch. Accordingly, automatic routing from microprocessor core 20 to FPGA 10 would be impracticable owing to design rule violations. To reduce such design rule violations with automatic routing, a neutral or compromise pitch set is employed.

[0023] Continuing the above example, reference is made to FIGS. 3A and 3B, where shown are line diagrams of respective exemplary portions of 30 and 31 of interconnect layers from FPGA 10 and microprocessor core 20, respectively, of FIG. 1. Grid portion 30 comprises vertical conductive lines 11 and horizontal conductive lines 12. Spacing between vertical conductive lines 11 is horizontal pitch H1, and spacing between horizontal conductive lines 12 is vertical pitch V1. Grid portion 31 comprises vertical conductive lines 21 and horizontal conductive lines 22. Spacing between vertical conductive lines 21 is horizontal pitch H2, and spacing between horizontal conductive lines 22 is vertical pitch V2. Continuing the above example, H1 and V1 are .66 microns and .60 microns, respectively, and H2 and V2 are each .57 microns.

[0024] Referring to FIG. 4, there is shown a cross-sectional diagram of exemplary portions of FPGA 10 and microprocessor core 20 of FIG. 1. FPGA 10 is shown with five interconnect layers 41, 42, 43, 44 and 45, though fewer or more interconnect layers may be used. Microprocessor core 20 is shown with three interconnect layers 51, 52 and 53, though fewer or more interconnect layers may be used. Region 15 may

comprise standard cells or a filler material, such as a dielectric, or a combination thereof.

[0025] Vias 16 are shown connecting pins 28 to conductive lines 11 and 12. Notably, pins 28 are conventionally connected to at least one of lines 21 and 22, though not shown here for purposes of clarity. Moreover, spacing or vertical pitch of pins 28 is V2, as shown in FIG. 1.

[0026] As shown, a compromise pitch is used for interconnect layers 42 and 44, namely, V2, which is the vertical pitch used for microprocessor core 20 conductive lines 22 and pins 28. However, interconnect layers 41, 43 and 45 use a horizontal pitch H1 from FPGA 10 layout. In this manner, interconnect layers 42 and 44 are on vertical pitch V2 with pins 28 for connection thereto. This facilitates connecting to pins 28 without off-line line routing, namely, routing in between conductive lines, and thus reduces likelihood of design rule spacing violations. Moreover, if pins 28 form a bus, multiple vias 16 may be used to connect to pins 28 to provide bus connectivity.

[0027] Notably, FPGA 10 retains horizontal pitch H1 for layers 41, 43 and 45. This facilitates not violating design rules for FPGA 10. Moreover, as conductive lines of interconnect layers 41, 43 and 45 are not parallel with conductive lines of interconnect layers 42 and 45, vias 16 may couple conductive lines 11 and 12 without violating design rules.

[0028] Referring to FIG. 5, there is shown a line diagram of an exemplary portion 50 of an interconnect layer from FPGA 10 in accordance with an aspect of the present invention. Conductive lines 12 have a vertical pitch of V2, and conductive lines 11 have a horizontal pitch of H1. However, depending on orientation of pins 28 of FIG. 1, H1 may need to be substituted for H2. Thus, the present invention may be used to provide a pitch set (V1, H2) for FPGA 10. Moreover, if both vertically and horizontally oriented pins are

present, then a plurality of interconnect layers of one pitch set (V1, H2) are used for the vertically oriented pins, and another plurality of interconnect layers of another pitch set (V2, H1) are used for the horizontally oriented pins.

[0029] Notably, substitution of either V1 or H1 with V2 or H2 for FPGA 10 layout and routing is used for interconnect layers, namely, layers for interconnecting microprocessor core 20 to FPGA 10. Though these interconnect layers may be used for FPGA location to FPGA location connectivity, other layers not used for interconnecting FPGA 10 to microprocessor core 20 may be present.

[0030] Referring to FIG. 6, there is shown a cross-sectional diagram of an exemplary portion of FPGA 10 and microprocessor core 20 in accordance with one or more aspects of the present invention. Metal layers 46, 47 and 48 are shown above interconnect layer 45. Metal layers 46, 47 and 48 comprise pitches H1 and V1. Use of FPGA 10 native pitches for non-interconnect layers to microprocessor core 20 facilitates automatic routing without design rule spacing violation.

[0031] Input to a conventional automatic routing program is done for each layer. With renewed reference to FIG. 5, inputs for an automatic routing program for each interconnect layer shown for FPGA 10 are set forth in Table I.

Layer Ref. No.	Pitch	Direction
41	H1	Vertical
42	V2	Horizontal
43	H1	Vertical
44	V2	Horizontal
45	H1	Vertical

Table I

[0032] Referring to FIG. 7, there is shown a flow diagram of an exemplary embodiment of a process 70 in accordance with

one or more aspects of the present invention. At step 71, pitch from a first device is obtained or determined. At step 72, pitch from a second device is obtained. At step 73, pitch from the first device and pitch from the second device are provided to a database accessible by a routing program. And, at step 74, the routing program is run using the pitch from the first device and the second device.

[0033] Though exemplary pitches were described above, it should be understood that the present invention is not so limited. Conventionally, horizontal and vertical pitches vary depending at least in part on lithography. However, it should be appreciated that the present invention scales with lithography, and thus the present invention may be employed in semiconductor processes for embedding a core device into another device where both devices are designed to be manufactured using submicron lithographic processes.

[0034] While foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow. For example, though the present invention is described in terms of an FPGA and embedded processor core, it should be understood that constructs other than an FPGA and an embedded processor core may be used, including, but not limited to, combinations formed from at least two of a programmable logic device, a memory, an Application Specific Integrated Circuit, an Application Specific Standard Product, a Digital Signal Processor, a microprocessor, a microcontroller, and the like.

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